GOC-BE440

Bluetooth Module Hardware Specification

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Be careful:

1. The module must use ladder steel net, and recommend ladder steel net thickness 0.16--0.20mm. The adaptability of the products is adjusted accordingly.

2. Before the use of the module, bake at 60 degrees centigrade and bake for 12 hours.

Release Record

Version Number	Release Date	Contents
V1.0	2019/05/17	Initial draft
V1.1	2019/08/30	Increase packing methods and performance parameters, Cancel reference design
V1.2	2020/08/19	Update Net Weight

Contents

1. Introduction

The GOC-BE440 is a monolithic, Bluetooth 5.0+EDR+BLE compliant,stand-alone baseband processor with an integrated 2.4GHz transceiver. Manufactured using the industry's most advanced 40nm CMOS low-power process, the GOC-BE440 employs the highest level of integration,eliminating all critical external components, and thereby minimizing the device's footprint and costs associated with the implementation of Bluetooth solutions.

The GOC-BE440 is the optimal solution for voice and data applications that require a Bluetooth SIG standard Host Controller Interface (HCI) via UART H4, and PCM audio interface support.

The GOC-BE440 transceiver's enhanced radio performance meets the most stringent industrial temperature application requirements for compact integration into mobile handset and portable devices.The GOC-BE440 provides full radio compatibility,enabling it to operate simultaneously with GPS and cellular radios.

1.1 Block Diagram

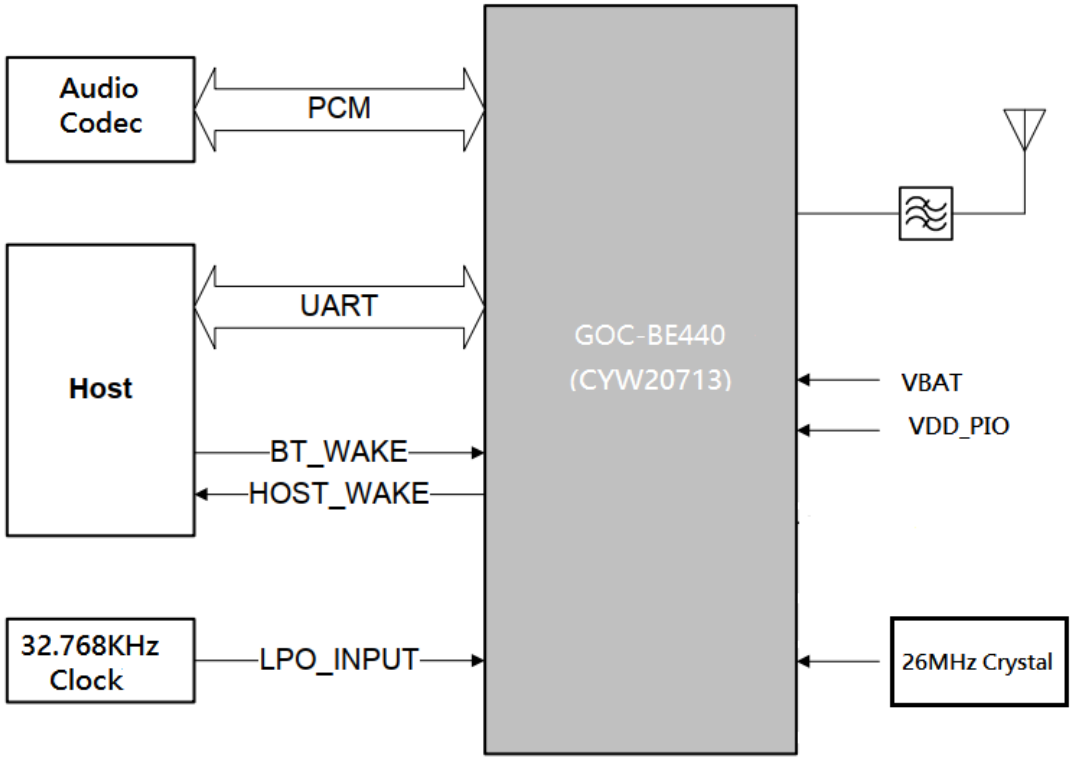


Figure 1: GOC-BE440 system Block Diagram

1.2 Features

- Bluetooth 5.0 + EDR compliant.
- Class 1 capable with built-in PA.
- Programmable output power control meets Class 1, Class 2 requirements.
- Use supply voltages up to 3.3V.Supports Cypress SmartAudio®, wide-band speech, SBC codec, and packet loss concealment.
- Fractional-N synthesizer supports frequency references from 12 MHz to 52 MHz.
- Automatic frequency detection for standard crystal and TCXO values when an external 32.768 kHz reference clock is provided.

- Ultra-low power consumption.
- Supports serial flash interfaces.
- ARM7TDMI-S–based microprocessor with integrated ROM and RAM.
- Supports patch RAM download without external memory.

1.2.1 Transmit And Receive Functions

The following transmit and receive functions are implemented in the BBC hardware to increase the reliability and security of the TX/RX data before sending the data over the air:
In the transmitter:

Data framing:

- Forward error correction (FEC) generation
- Header error control (HEC) generation
- Cyclic redundancy check (CRC) generation
- Key generation
- Data encryption
- Data whitening

In the receiver:

- Symbol timing recovery
- Data deframing
- FEC
- HEC
- CRC
- Data decryption
- Data dewhitening

1.2.2 Bluetooth 5.0 + EDR Features

The GOC-BE440 supports Bluetooth5.0 + EDR, including the following options:

- Whitelist size of 25
- Enhanced Power Control
- HCI Read Encryption Key Size command

The GOC-BE440 provides full support for Bluetooth 2.1 + EDR additional features:

- Secure simple pairing (SSP)
- Encryption pause resume (EPR)
- Enhance inquiry response (EIR)
- Link supervision time out (LSTO)
- Sniff subrating (SSR)
- Erroneous data (ED)
- Packet boundary flag (PBF)

1.3 Applications

- Automotive handsfree radios
- Automotive data communication
- Industrial appliances

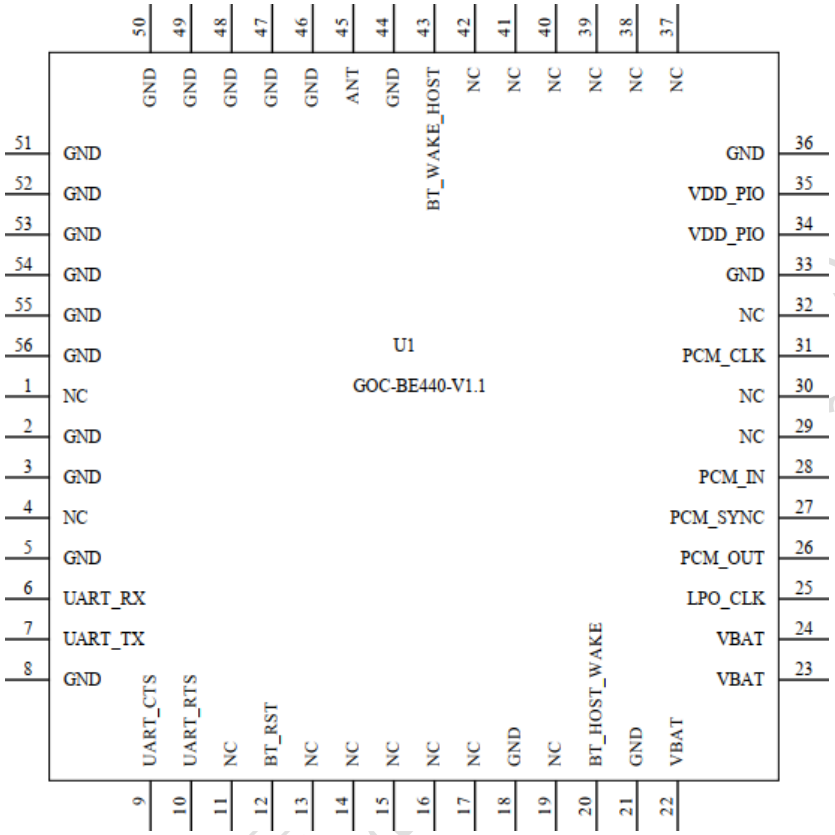
2. Main Specification Instruction

Production	**Bluetooth Module**
Type	GOC-BE440
Standard	Bluetooth V5.0+EDR+BLE
Frequency Range	2402~2480MHz
Modulation Method	GFSK、 π/4 DQPSK、8DPSK
Max Speed ForTransfer	Asynchronous: 723.2kbps/57.6kbps Synchronous: 433.9kbps/433.9kbps
Hop	1600hops/sec, 1MHz channel space
Output Impedance	50 ohms
Crystal Frequency	26MHz
Outer Interface	Power,UART,PCM
Apply To Bluetooth Instructions	A2DP, AVRCP,PBAP,HID,BLE, ,HS/HF ,SPP
Range For Working Distance	10 meters (33 files)
Receiving Sensitivity	-90dBm
Emissive Power	<10 dBm
Connect Method	Point to Multi-Point
Size	17.0*17.0*2.4mm(L*W*H)
Power Voltage	3.30V Supply Voltage
Working Current	<44mA
Standby Current	<730uA
Working Temperature	-40℃ to +85℃
Storage Temperature	-40℃ to +125℃
Humidity Range	10%~90% Non-Condensing

Table 1: Main Specifications

3. Pin Diagram And Description

3.1 Pin Diagram



Figur 2: GOC-BE440 Pin Diagram

3.2 Pin Description

Pin	Pin Name	**Type**	Description
1	NC	NC	No connect
2	GND	Ground	Ground
3	GND	Ground	Ground
4	NC	NC	No connect
5	GND	Ground	Ground
6	UART_RX	Input	BT UART Data Input
7	UART_TX	Output	BT UART Data Output
8	GND	Ground	Ground
9	UART_CTS	Input	UART CTS
10	UART_RTS	Output	UART RTS
11	NC	NC	NC

12	BT_RST	Input	Active-low reset input
13	NC	NC	No connect
14	NC	NC	No connect
15	NC	NC	No connect
16	NC	NC	No connect
17	NC	NC	No connect
18	GND	Ground	Ground
19	NC	NC	No connect
20	BT_HOST_WAKE	Input/Output	Bluetooth device to wake-up HOST(Reserved)
21	GND	Ground	Ground
22	VBAT	POWER	3.3V Supply Voltage
23	VBAT	POWER	3.3V Supply Voltage
24	VBAT	POWER	3.3V Supply Voltage
25	LPO_32K	Input	External LPO input
26	PCM_OUT	Output	PCM data Out
27	PCM_SYNC	Input/Output	PCM Synchronization control
28	PCM_IN	Input	PCM data Input
29	NC	NC	No connect
30	NC	NC	No connect
31	PCM_CLK	Input/Output	PCM Clock
32	NC	NC	No connect
33	GND	Ground	Ground
34	VDD_PIO	POWER	1.8V~3.3VSupply Voltage
35	VDD_PIO	POWER	1.8V~3.3V Supply Voltage
36	GND	Ground	Ground
37	NC	NC	No connect
38	NC	NC	No connect
39	NC	NC	No connect
40	NC	NC	No connect
41	NC	NC	No connect
42	NC	NC	No connect
43	BT_WAKE_HOST	Input/Output	HOST wake-up Bluetooth device(Reserved)
44	GND	Ground	Ground

45	ANT	RF	Bluetooth Antenna(Reserved)
46	GND	Ground	Ground
47	GND	Ground	Ground
48	GND	Ground	Ground
49	GND	Ground	Ground
50	GND	Ground	Ground
51	GND	Ground	Ground
52	GND	Ground	Ground
53	GND	Ground	Ground
54	GND	Ground	Ground
55	GND	Ground	Ground
56	GND	Ground	Ground

Table 2: Pin Description

3.3 PCB Layout Footprint

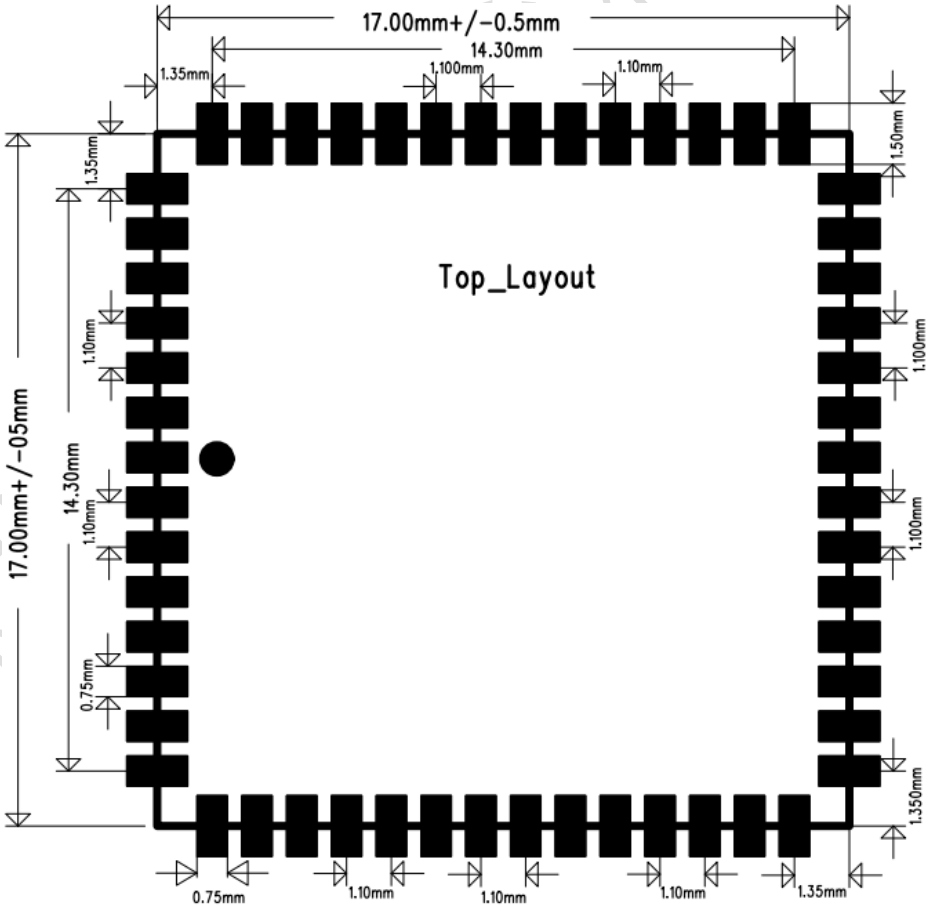


Figure 3: PCB Layout Footprint

6.4 Module Package

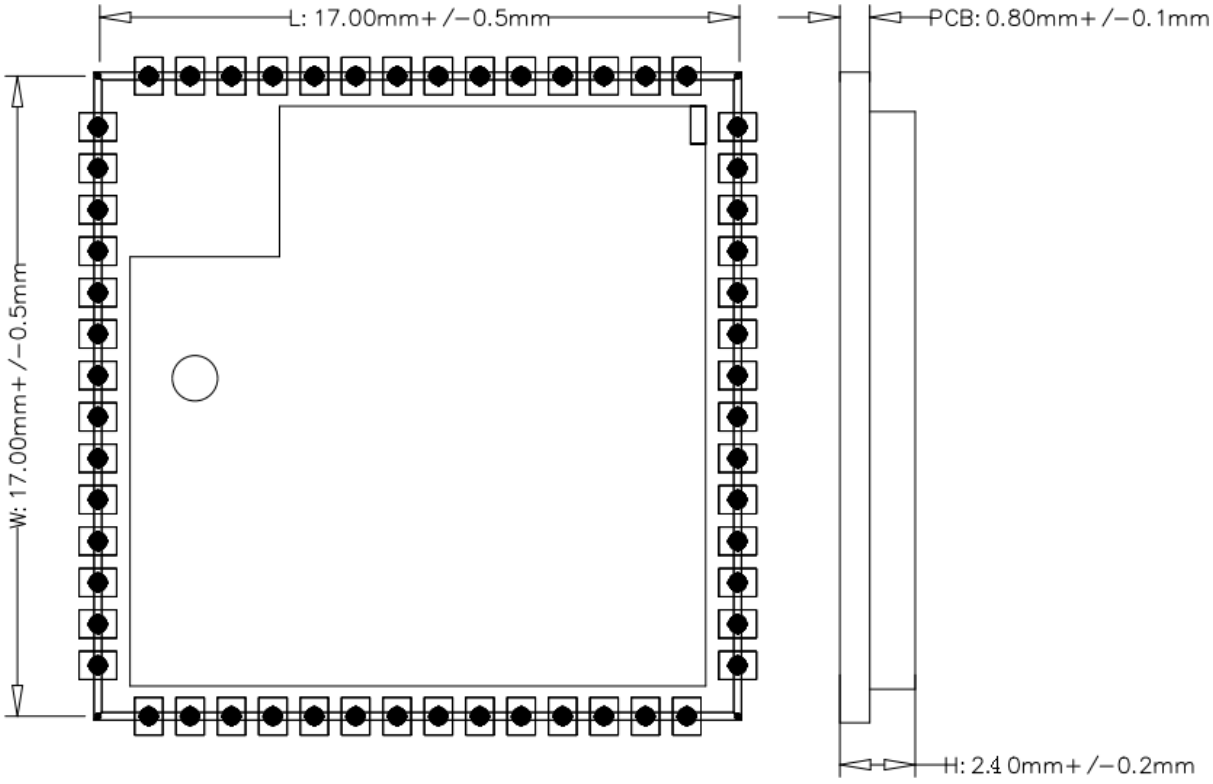


Figure 4: Module Package

4. Approximate Dimensions Of Inverted-F Antenna

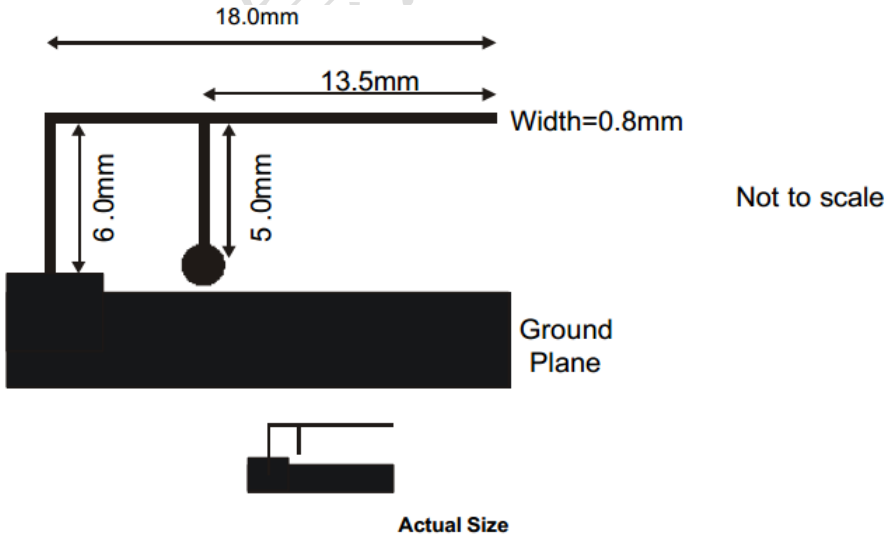


Figure 5: Approximate Dimensions Of Inverted-F Antenna

Special attention：

1.The position of the Bluetooth module is as far as possible not to walk the line and to lay the copper, especially in the vicinity of the antenna position.

2.Usually the Bluetooth module of the antenna as close to the edge of the PCB position, PCB antenna position slot.

3. In order to make the antenna performance in good condition, the antenna transmission line as far as possible in a straight line, the antenna on the top or bottom, do not play over the hole, the antenna and the distance between the laying of copper is greater than two times the normal spread of copper

4. Antenna transmission line to the length of the line should be as short as possible, should go to the surface, the length of the antenna is generally 30mm.

5. RF Interface

The module integrates a balun filter. A 50ohms load is needed.

6. Peripheral Transport Unit

This section discusses the PCM, UART, and SPI peripheral interfaces. The GOC-BE440 has a 1040 byte transmit and receive FIFO, which is large enough to hold the entire payload of the largest EDR BT packet (3-DH5).

6.1 Power Sequence

6.1 .1 Power On Sequence

VBAT should not raise 10%-90%faster than 40 microseconds or slower than 10milliseconds.
VBAT should be up before or at the same time as VDD_PIO. VDD_PIO should NOT be present fast or be held high before VBAT is high.
BT_RST should be up after sleep clock oscillation is stabilized.
Please keep repeats power off sequence and power on sequence several times until it started normally.

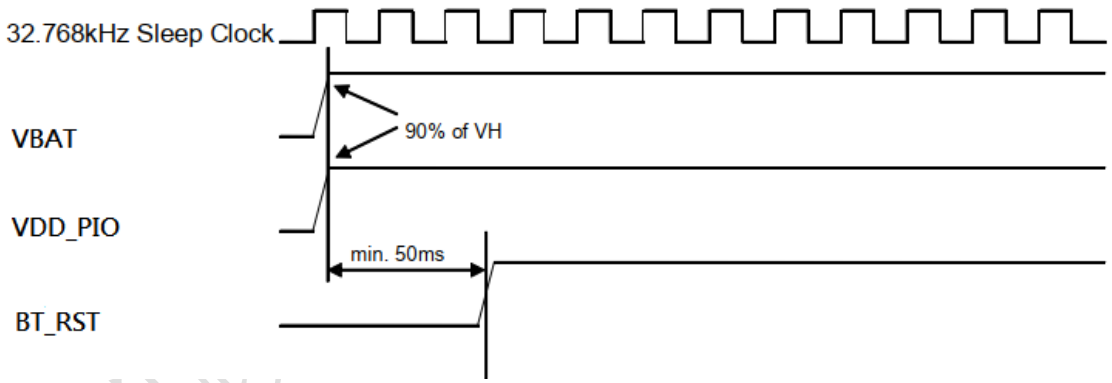


Figure 6: Power On Sequence

Note
1) The GOC-BE440 has an internal Power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VBAT and VDD_PIO have both passed the POR threshold. Wait at least 150 ms after VBAT and VDD_PIO are available before initiating UART accesses.
2) VBAT should not rise 0% faster than 40 microseconds. VBAT should be up before or at the same time as VDD_PIO should NOT be present first or be held high before VBAT is high.
3) After VBAT/VDD_PIO is turned off, keep VBAT/VDD_PIO OFF for at least 30 ms until next VBAT/VDD_PIO ON.

6.1.2 Power Down Sequence

VDD_PIO should be down before or at the same time as VBAT. VBAT should NOT be down earlier than VDD_PIO low.
VDD_PIO becomes low state is prior to VBAT low.
VBAT and VDD_PIO should be down after BT_RST are low. Waiting time from RST down to power supply off is not prescribed.

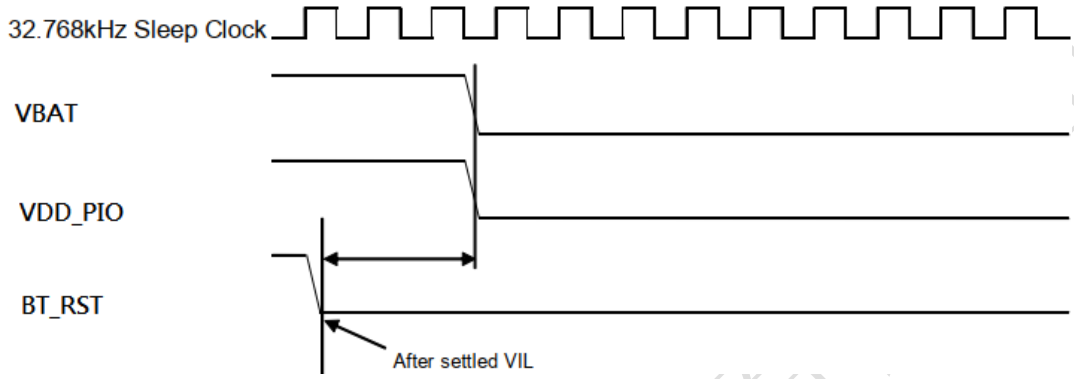


Figure 7: Power Down Sequence

6.2 PCM Interface

The GOC-BE440 PCM interface can connect to linear PCM codec devices in master or slave mode. In master mode, the device generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface as inputs to the device.

The device supports up to three SCO or eSCO channels through the PCM interface and each channel can be independently mapped to any available slot in a frame.

The host can adjust the PCM interface configuration using vendor-specific HCI commands or it can be setup in the configuration file.

6.2.1 System Diagram

Figure 8 shows options for connecting the device to a PCM codec device as a master or a slave.

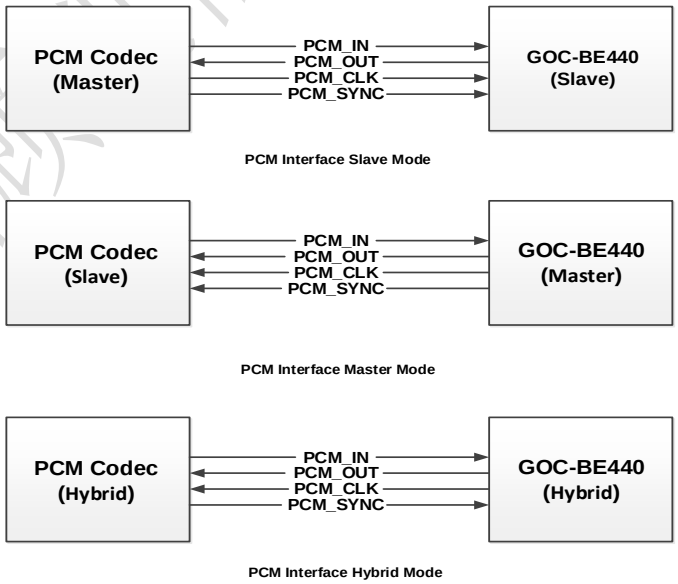


Figure 8: PCM Interface with Linear PCM Codec

6.2.2 Slot Mapping

The device supports up to three simultaneous, full-duplex SCO or eSCO channels. These channels are time-multiplexed onto the PCM interface using a time slotting scheme based on the audio sampling rate, as described in Table 3.

Audio Sample Rate	Time Slotting Scheme
8 kHz	The number of slots depends on the selected interface rate, as follows: **Interface rate Slot** 128 1 256 2 512 4 1024 8 2048 16
16 kHz	The number of slots depends on the selected interface rate, as follows: **Interface rate Slot** 256 1 512 2 1024 4 2048 8

Table 3: PCM Interface Time Slotting Scheme

Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

6.2.3 Wideband Speech

The GOC-BE440 provides support for wideband speech (WBS) in two ways:

■ Transparent mode: The host encodes WBS packets and the encoded packets are transferred over the PCM bus for SCO or eSCO voice connections. In Transparent mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate.

■ On-chip SmartAudio® technology: The GOC-BE440 can perform Subband-Codec (SBC) encoding and decoding of linear 16 bits at 16 kHz (256 kbps rate) transferred over the PCM bus.

6.2.4 Frame Synchronization

The device supports both short and long frame synchronization types in both master and slave configurations. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the 8 kHz audio frame rate (which is a single bit period in width) and synchronized to the rising edge of the bit clock. The PCM slave expects PCM_SYNC to be high on the falling edge of the bit clock and the first bit of the first slot to start at the next rising edge of the clock. In the long frame synchronization mode, the frame synchronization signal is an active-high pulse at the 8 kHz audio frame rate. However, the duration is 3-bit periods and the pulse starts coincident with the first bit of the first slot.

6.2.5 Data Formatting

The device can be configured to generate and accept several different data formats. The device uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits is configurable to support various data formats on the PCM interface. The remaining three bits are ignored on the input, and may be filled with zeros, ones, a sign bit, or a programmed value on the output. The default format is 13-bit two's complement data, left justified, and clocked most significant bit first.

6.3 PCM Interface Timing

Reference	Characteristics	Minimum	Maximum	Unit
1	PCM bit clock frequency	128	2048	kHz
2	PCM bit clock HIGH time	128	–	ns
3	PCM bit clock LOW time	209	–	ns
4	Delay from PCM_CLK rising edge to PCM_SYNC high	–	50	ns
5	Delay from PCM_CLK rising edge to PCM_SYNC low	–	50	ns
6	Delay from PCM_CLK rising edge to data valid on PCM_OUT	–	50	ns
7	Setup time for PCM_IN before PCM_CLK falling edge	50	–	ns
8	Hold time for PCM_IN after PCM_CLK falling edge	10	–	ns
9	Delay from falling edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance	–	50	ns

Table 4: PCM Interface Timing Specifications (Short Frame Synchronization, Master Mode)

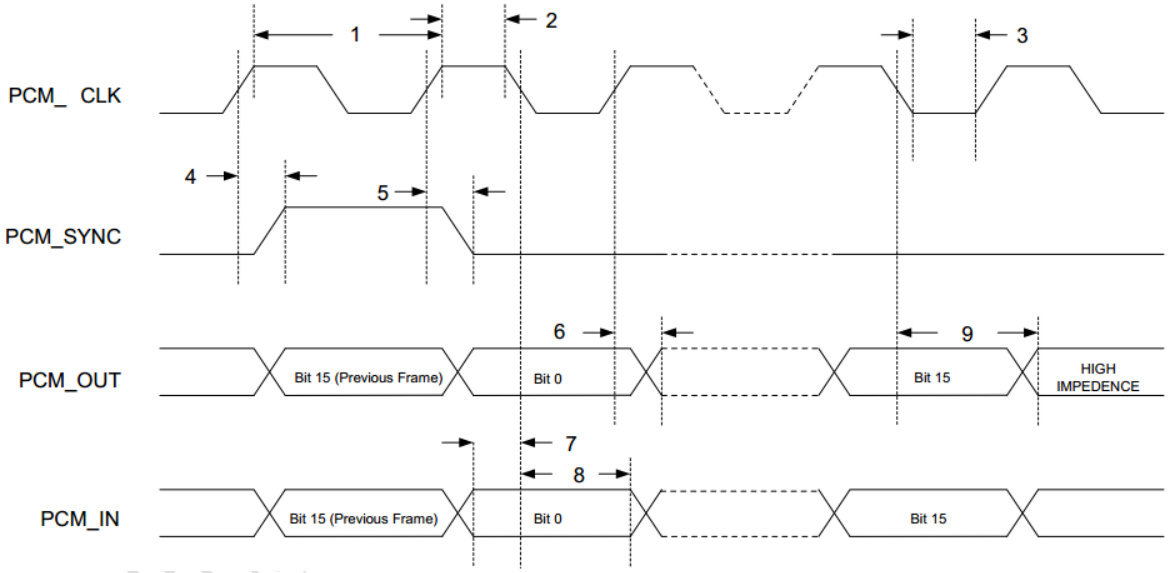


Figure 9: PCM Interface Timing (Short Frame Synchronization, Master Mode)

Reference	Characteristics	Minimum	Maximum	Unit
1	PCM bit clock frequency	128	2048	kHz
2	PCM bit clock HIGH time	209	–	ns
3	PCM bit clock LOW time	209	–	ns
4	Setup time for PCM_SYNC before falling edge of PCM_CLK	50	–	ns
5	Hold time for PCM_SYNC after falling edge of PCM_CLK	10	–	ns
6	Hold time of PCM_OUT after PCM_CLK falling edge	–	175	ns
7	Setup time for PCM_IN before PCM_CLK	50	–	ns

	falling edge			
8	Hold time for PCM_IN after PCM_CLK falling edge	10	–	ns
9	Delay from falling edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance	–	100	ns

Table 5: PCM Interface Timing Specifications (Short Frame Synchronization, Slave Mode)

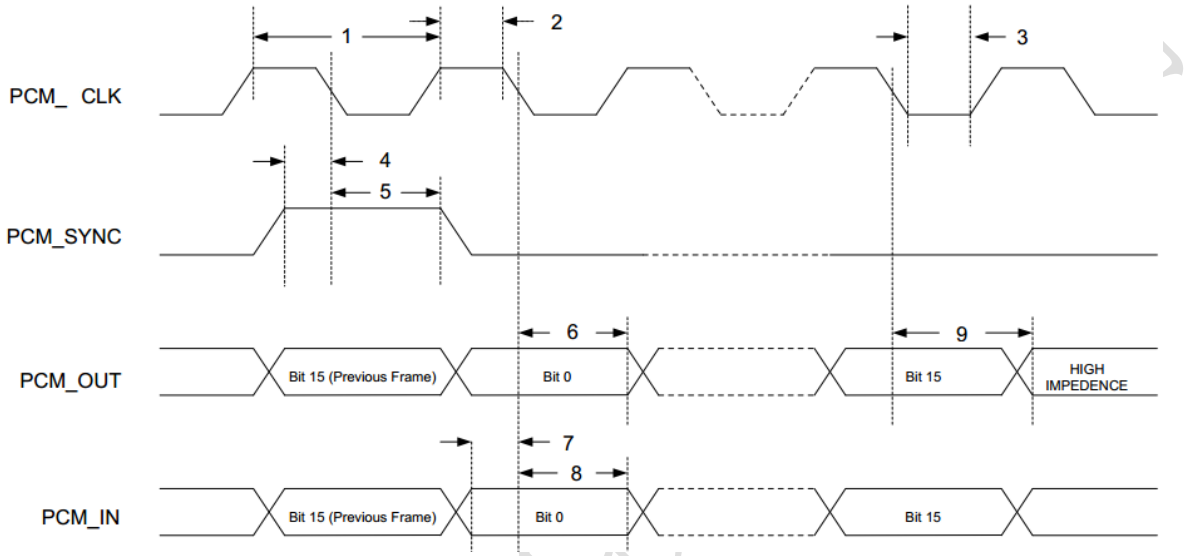


Figure 10: PCM Interface Timing (Short Frame Synchronization, Slave Mode)

Reference	Characteristics	Minimum	Maximum	Unit
1	PCM bit clock frequency	128	2048	kHz
2	PCM bit clock HIGH time	209	–	ns
3	PCM bit clock LOW time	209	–	ns
4	Delay from PCM_CLK rising edge to PCM_SYNC HIGH during first bit time	–	50	ns
5	Delay from PCM_CLK rising edge to PCM_SYNC LOW during third bit time	–	50	ns
6	Delay from PCM_CLK rising edge to data valid on PCM_OUT	–	50	ns
7	Setup time for PCM_IN before PCM_CLK falling edge	50	–	ns
8	Hold time for PCM_IN after PCM_CLK falling edge	10	–	ns
9	Delay from falling edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance	–	50	ns

Table 6: PCM Interface Timing Specifications (Long Frame Synchronization, Master Mode)

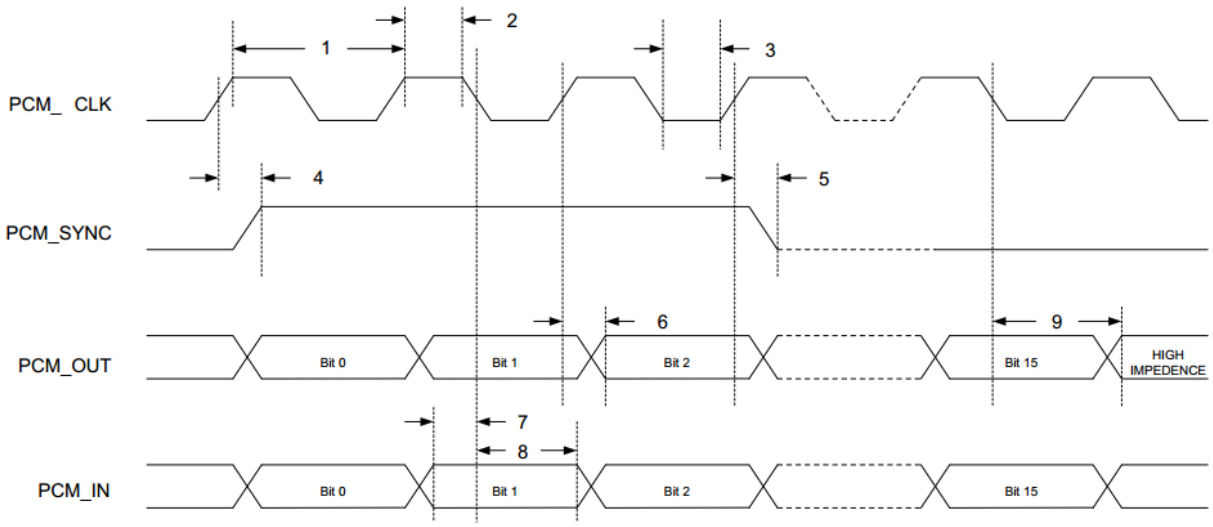


Figure 11: PCM Interface Timing (Long Frame Synchronization, Master Mode)

Reference	Characteristics	Minimum	Maximum	Unit
1	PCM bit clock frequency.	128	2048	kHz
2	PCM bit clock HIGH time.	209	–	ns
3	PCM bit clock LOW time.	209	–	ns
4	Setup time for PCM_SYNC before falling edge of PCM_CLK during first bit time.	50	–	ns
5	Hold time for PCM_SYNC after falling edge of PCM_CLK during second bit period. (PCM_SYNC may go low any time from second bit period to last bit period).	10	–	ns
6	Delay from rising edge of PCM_CLK or PCM_SYNC (whichever is later) to data valid for first bit on PCM_OUT.	–	50	ns
7	Hold time of PCM_OUT after PCM_CLK falling edge.	–	175	ns
8	Setup time for PCM_IN before PCM_CLK falling edge.	50	–	ns
9	Hold time for PCM_IN after PCM_CLK falling edge.	10	–	ns
10	Delay from falling edge of PCM_CLK or PCM_SYNC (whichever is later) during last bit in slot to PCM_OUT becoming high impedance.	–	100	ns

Table 7: PCM Interface Timing Specifications (Long Frame Synchronization, Slave Mode)

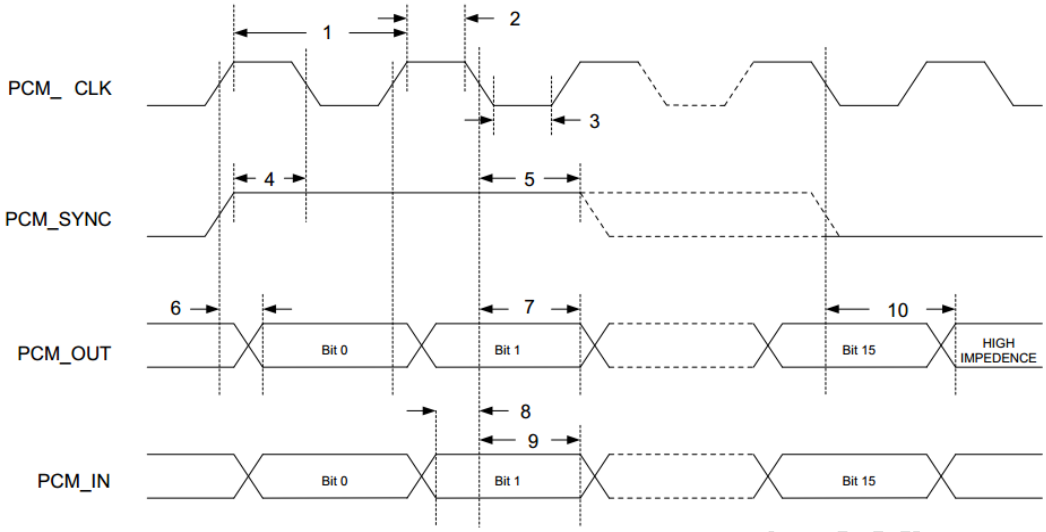


Figure 12: PCM Interface Timing (Long Frame Synchronization, Slave Mode)

7. UART Interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate can be selected via a vendor-specific UART HCI command. The interface supports Bluetooth UART HCI (H4) specifications. The default baud rate for H4 is 115.2 Kbaud.

The following baud rates are supported:

■ 9600	■ 115200	■ 2000000
■ 14400	■ 230400	■ 3000000
■ 19200	■ 460800	■ 3250000
■ 28800	■ 921600	■ 3692000
■ 38400	■ 1444444	■ 4000000
■ 57600	■ 1500000	

Table 8: Example of Common Baud Rates

Normally, the UART baud rate is set by a configuration record downloaded after reset or by automatic baud rate detection. The host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is provided through a vendor-specific command.

The GOC-BE440 UART operates with the host UART correctly, provided the combined baud rate error of the two devices is within ±2%.

When connecting the module to a host, please make sure to follow Figure13.

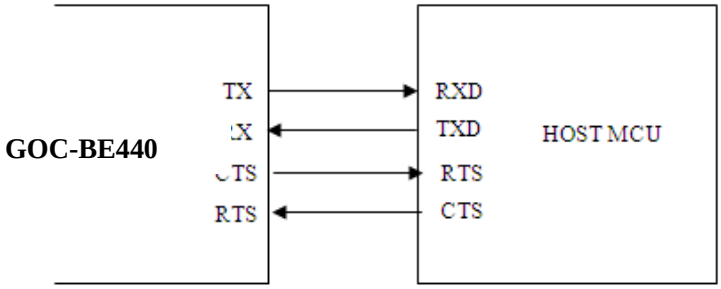


Figure 13: GOC-BE440 and HOST MCU use UART interface

7.1 UART Timing

Reference	Characteristics	Minimum	Maximum	Unit
1	Delay time, UART_CTS low to UART_TX valid	–	24	Baudout cycles
2	Setup time, UART_CTS high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS high	–	2	Baudout cycles

Table 9: UART Timing Specifications

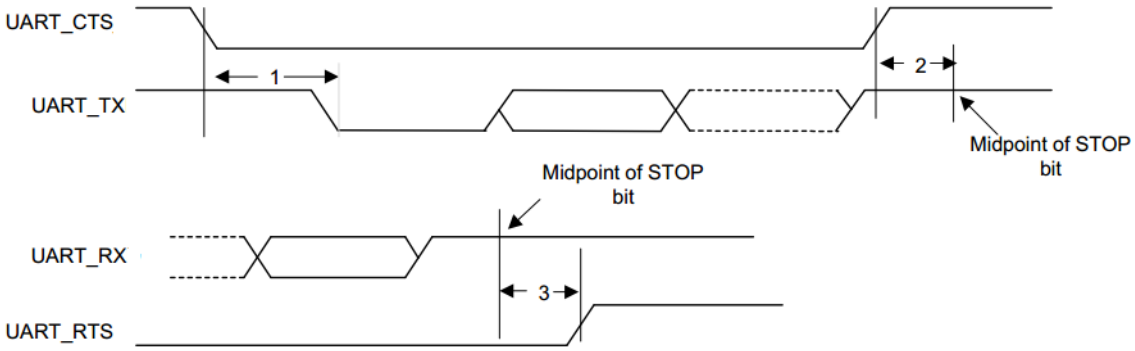


Figure 14: UART Timing

8. LPO Clock Interface

The LPO clock is the second frequency reference that the GOC-BE440 uses to provide low-power mode timing for park, hold, and sniff. The LPO clock can be provided to the device externally, from a 32.768 kHz source or the GOC-BE440 can operate using the internal LPO clock.

The LPO can be internally driven from the main clock. However, sleep current will be impacted.

The accuracy of the internal LPO limits the maximum park, hold, and sniff intervals.

Parameter	External LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Input signal amplitude	200 to 3600	mVp-p
Signal type	Square-wave or sine-wave	–
Input impedance (when power is applied or power is off)	>100 <5	kΩ pF

Table 10: External LPO Signal Requirements

9. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : ≦260 ℃

Number of Times : 2 times

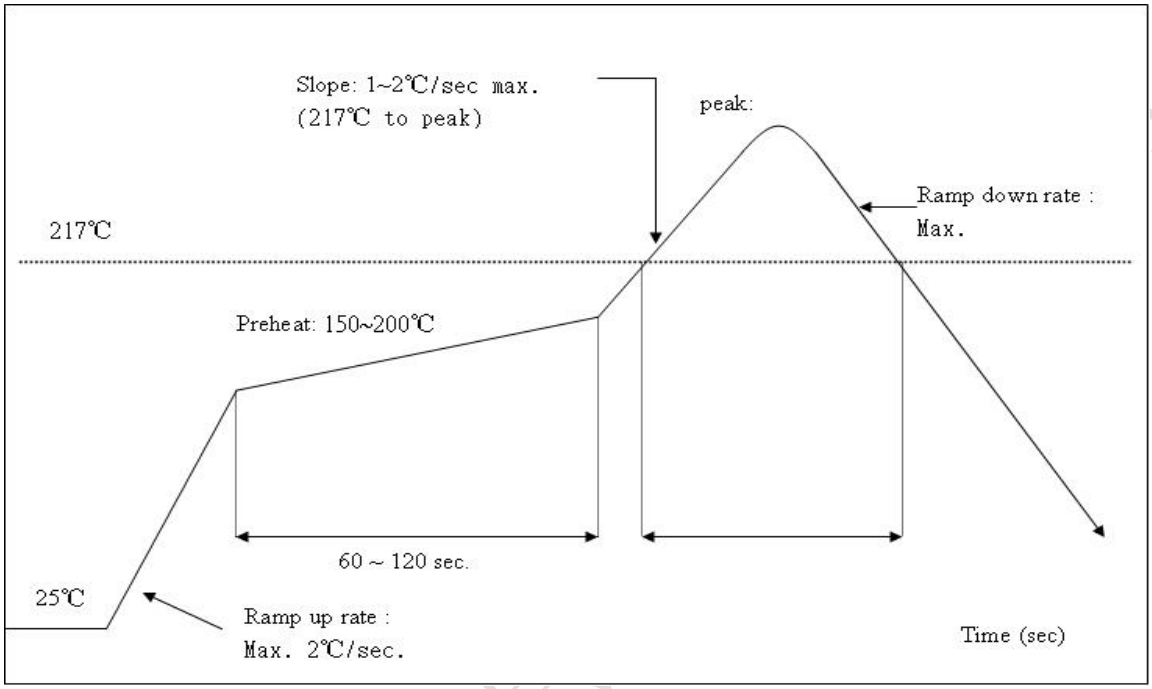


Figure 15: Solder Reflow Profile

10. Electrical Characteristics

10.1 Absolute Maximum Ratings

Rating	Min	Typical	Max
VBAT	1.7V	3.3V	3.6V
VDD_PIO	1.7V	-	3.6V

Table 11: Absolute Maximum Ratings

10.2 Recommended Operating Conditions

Operating Condition	Min	Typical	Max
Storage Temperature	-40 ℃	-	+125 ℃
OperatingTemperature	-40 ℃	-	+85 ℃
VBAT	3.13V	3.30V	3.46V
VDD_PIO	1.71V	1.80V	1.89V
	3.13V	3.30V	3.46V

Table 12: Recommended Operating Conditions

11. PCB Layout Recommendation

11.1 Antenna

Antenna trace impedance should be adjusted to 50ohm.The area above(or under)the RF antenna trace should be free from other traces.

11.2 HCI UART Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA
UART_RX UART_TX UART_CTS UART_RTS
The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

11.3 PCM Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 mA
PCM_SYNC PCM_CLK PCM_OUT PCM_IN
The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

11.4 Power Trace Lines Layout Guideline

- VBAT Trace Width: 20mil
- VDD_PIO Trace Width: 20mil

11.5 Ground Lines Layout Guideline

- A Complete Ground in Ground Layer.
- Add Ground Through Holes to GOC-BE440 Module Ground Pads
- Decoupling Capacitors close to GOC-BE440 Module Power and Ground Pads

12. Echo Cancellation Principle

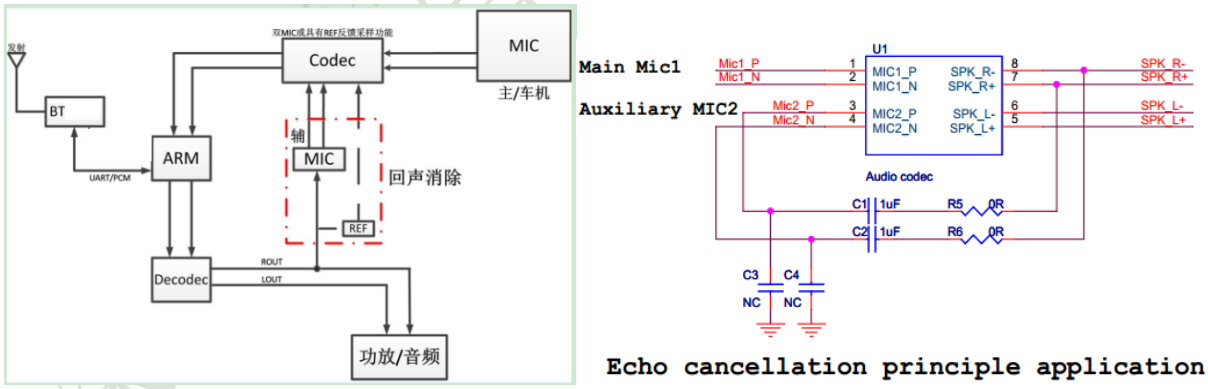


Figure 16: Sound processing flow chart

The left picture is a schematic diagram of the echo cancellation principle. After Decodec decoding of the left and right channel sound, after data sampling and master MIC data comparison, echo cancellation can be processed. The right picture is a reference example, which can be designed according to the actual plan. Flying echo cancellation design, priority to use the echo cancellation design of IFLYTEK.

13. Module Part Number Description

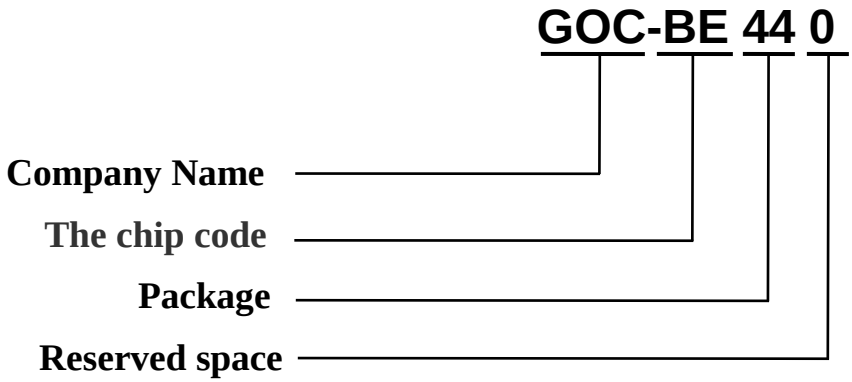


Figure 17: Module Part Number Description

For a list of available options (e.g. package, packing) and orderable part numbers or for further information on any aspect of this device, please go to www.goodocom.com or contact the GOODOCOM Sales Office nearest to you.

14. Ordering Information

Part Number	Description	Remark
GOC-BE440 V1.1	Bluetooth Module	

Table 13: Ordering Iinformation

15. Packaging Information

15.1 Net Weight

The module net weight: 1.3g±0. 2g

15.2 Package

72pcs module in one tray 2000pcs modules into one pack 4000pcs
Modules One Box Carton size:270mm*275mm*220mm
Tray size:225mm*205mm*7mm

15.3 Storage Requirements

1）Temperature: 22~28℃;
2）Humidity: <70%（RH）;
Vacuum packed and sealed in good condition to ensure 12 months of welding.

15.4 Humidity Sensitive Characteristic

1） MSL: 3 level

2） Once opened, SMT within 168 hours in the condition of temperature: 22~28℃ and humidity<60%(RH).

3） Handling, storage, and processing should follow IPC/JEDECJ-STD-033